AMENDMENTS TO THE CLAIMS

The claims are presented below with their amendment status and revision marks to indicate any amendments.

1. (CURRENTLY AMENDED) A method comprising:

requesting a strobe signal from a transmitting device, if no strobe signal has been received within a pre-determined time period;

generating a clock signal aligned relative to an edge of ~~a~~ the strobe signal~~; received from a transmitting device;~~ and

latching one or more data signals received from the transmitting device using the clock signal.

2. (CURRENTLY AMENDED) The method of claim 1, wherein the clock signal is not edge aligned with the strobe signal. ~~the generating the clock signal comprises substantially aligning an edge of the clock signal with an edge of a strobe signal and delaying the clock signal by a predetermined amount of time.~~

3. (CURRENTLY AMENDED) The method of claim 1, wherein the method comprises generating one or more latch control signals aligned relative to the clock signal; and

wherein the latching comprises latching one or more data signals received from the transmitting device with the one or more latch control signals.

4. (CURRENTLY AMENDED) The method of claim 3, wherein the generating the clock signal comprises substantially aligning an edge of the clock signal with an edge of ~~a~~ the strobe signal; and

wherein the generating one or more latch control signals comprises substantially aligning an edge of one or more latch control signals relative to ~~with~~ an edge of the clock signal, wherein the latch control signals and the clock signal are not edge aligned. ~~and delaying one or more latch control signals by a predetermined amount of time.~~

5. (ORIGINAL) The method of claim 3, wherein the latching comprises latching a first set of a plurality of data signals with a first latch control signal and latching a second set of a plurality of data signals with a second latch control signal.

6. (CURRENTLY AMENDED) The method of claim 1, ~~comprising receiving from the transmitting device a~~ wherein the strobe signal ~~defining~~ is a pulse having a first edge associated with a first set of one or more data signals and a second edge associated with a second set of one or more data signals.

7. (CURRENTLY AMENDED) The method of claim ~~1, comprising transmitting a request to the transmitting device to receive a strobe signal for alignment of the clock signal after a strobe signal has not been received for a predetermined time interval.~~ 3, wherein the latch control signals are phase delayed from the strobe signal.

8. (CURRENTLY AMENDED) An apparatus comprising:

clock generation circuitry to generate a clock signal aligned relative to an edge of a strobe signal received from a transmitting device, wherein the apparatus requests the strobe signal from the transmitting device if no strobe signal has been received within a pre-determined time period;

control signal generation circuitry to generate one or more latch control signals aligned relative to an edge of the clock signal; and

latching circuitry to latch one or more data signals received from the transmitting device with one or more latch control signals.

9. (CURRENTLY AMENDED) The apparatus of claim 8, wherein the clock signal is not edge-aligned with the strobe signal. ~~the clock generation circuitry comprises circuitry to substantially align an edge of the clock signal with an edge of a strobe signal and circuitry to delay the clock signal by a predetermined amount of time.~~

10. (CURRENTLY AMENDED) The apparatus of claim 8, wherein the clock signal is substantially edge aligned with the strobe signal; and ~~generation circuitry comprises circuitry to substantially align an edge of the clock signal with an edge of a strobe signal; and~~

wherein the control signal generation circuitry ~~comprises circuitry to substantially align an edge of one or more latch control signals with an edge of the clock signal and circuitry to delay one or more latch control signals by~~

~~a predetermined amount of time~~ generates one or more latch control signals that are not edge-aligned with the clock signal.

11. (CURRENTLY AMENDED) The apparatus of claim 8, wherein the ~~clock generation circuitry is to receive from the transmitting device a~~ strobe signal ~~defining~~ is a pulse having a first edge associated with a first set of one or more data signals and a second edge associated with a second set of one or more data signals.

12. (ORIGINAL) The apparatus of claim 8, wherein the latching circuitry comprises a first latch to latch a first set of a plurality of data signals with a first latch control signal and a second latch to latch a second set of a plurality of data signals with a second latch control signal.

13. (CURRENTLY AMENDED) The apparatus of claim 8, comprising clock alignment control circuitry to request the strobe signal. ~~to receive a strobe signal for alignment of the clock signal.~~

14. (ORIGINAL) The apparatus of claim 13, wherein the clock alignment control circuitry comprises a counter to maintain a count to track time and a comparator to compare the count to a predetermined time interval.

15. (CURRENTLY AMENDED) An apparatus comprising:

means for aligning a clock signal ~~with~~ relative to a strobe signal, wherein the apparatus requests the strobe signal from a transmitting device if no strobe signal has been received within a pre-determined time period; and

means for latching one or more data signals using the clock signal.

16. (CURRENTLY AMENDED) The apparatus of claim 15, ~~comprising means for delaying the clock signal~~ wherein the clock signal and the strobe signal are not edge-aligned.

17. (CURRENTLY AMENDED) The apparatus of claim 15, comprising means for generating one or more latch control signals aligned relative to ~~with~~ the clock signal.

18. (CURRENTLY AMENDED) The apparatus of claim 17, ~~comprising means for delaying one or more latch control signals~~ wherein the latch control signals are not edge aligned with the strobe signal.

19. (CURRENTLY AMENDED) The apparatus of claim 15, comprising means for requesting the ~~a~~ strobe signal ~~to align the clock signal~~.

20. (CURRENTLY AMENDED) A system comprising:

one or more processors;

one or more memory modules; and

a memory controller coupled to one or more processors and to one or more memory modules, the memory controller having data signal reception latch control using a clock aligned relative to a strobe signal received from a memory module, wherein the memory controller requests the strobe signal if no strobe signal has been received within a pre-determined time period.

21. (CURRENTLY AMENDED) The system of claim 20, wherein the memory controller comprises respective latch control circuitry for each of a plurality of strobe signal lines for the one or more memory modules, each latch control circuitry comprising clock generation circuitry to generate a clock signal aligned relative to an edge of a strobe signal received from the respective strobe signal line and control signal generation circuitry to generate one or more latch control signals aligned relative to an edge of the clock signal.

22. (CURRENTLY AMENDED) The system of claim 21, wherein the clock signal and the strobe signal are not edge-aligned. ~~the clock generation circuitry comprises circuitry to substantially align an edge of the clock signal with an edge of a strobe signal and circuitry to delay the clock signal by a predetermined amount of time.~~

23. (CURRENTLY AMENDED) The system of claim 21, wherein the clock signal and the strobe signal are substantially edge-aligned, wherein the one or more latch control signals are not edge-aligned with the clock signal

~~clock generation circuitry comprises circuitry to substantially align an edge of the clock signal with an edge of a strobe signal; and~~

~~wherein the control signal generation circuitry comprises circuitry to substantially align an edge of one or more latch control signals with an edge of the clock signal and circuitry to delay one or more latch control signals by a predetermined amount of time.~~

24. (CURRENTLY AMENDED) The system of claim 21, wherein the memory controller comprises latching circuitry to latch one or more data signals received from one or more memory modules with the one or more latch control signals.

25. (CURRENTLY AMENDED) The system of claim 20, wherein the memory controller comprises respective clock alignment control circuitry for each of a plurality of strobe signal lines for one or more memory modules, wherein each clock alignment control circuitry ~~to request~~ requests to receive ~~a~~ an associated strobe signal over the respective strobe signal line for alignment of ~~a~~ an associated clock signal, if no associated strobe signal has been received within a pre-determined time period.

26. (CURRENTLY AMENDED) The system of claim 20, wherein one or more memory modules comprise double data rate dynamic random access memory (DDR DRAM).